



Advance Information

MPC603/MPC604 Evaluation System— Big Bend Technical Summary

This document describes an evaluation system that demonstrates the capabilities of two PowerPC™ microprocessors—the MPC603 or MPC604. The system, named Big Bend, is a PowerPC Reference Platform (PReP) compliant design. The motherboard inside the Big Bend system is an 8-layer PCB design, baby AT-size (9-inch x 13-inch) form factor, and uses the MPC105 processor to PCI bridge device for core logic. Other major components on the motherboard include the UMC PCI-ISA bridge, National Semiconductor's Super I/O controllers, and NCR's SCSI controller. Big Bend provides an example that can be used in designing other systems using PowerPC microprocessors. In addition to the Big Bend evaluation system, an evaluation kit containing design information and a manufacturing kit containing in-depth manufacturing information are available.

1.1 System Features

The main features of the Big Bend system are as follows:

- PReP compliant MPC603/MPC604 evaluation system
- Desktop system in baby AT form factor
- Supports MPC603 and MPC604 with external bus speeds up to 66 MHz
- Processor to PCI bridge with Motorola MPC105
- PCI to ISA bridge with UMC UM8886
- Onboard National Semiconductor PC87323 super I/O chip supports two 16550 serial ports, one parallel port, floppy, keyboard, mouse, and IDE interface

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MOTOROLA

- Onboard NCR53C825 SCSI controller to support the SCSI hard drive and CD ROM
- High performance PCI graphics
- Second-level cache selectable between 256 Kbyte, 512 Kbyte or 1 Mbyte
- Supports onboard DRAM up to 128 Mbyte; support for 4-Mbyte, 8-Mbyte, 16-Mbyte, and 32-Mbyte SIMMs
- Three 16-bit ISA bus slots and three 32-bit PCI bus slots
- Standard 101 PS/2™-style keyboard
- Supplied with Windows NT™ operating system and selected applications pre-installed on hard drive

1.2 System Block Diagram

Figure 1 shows the block diagram for the Big Bend motherboard:

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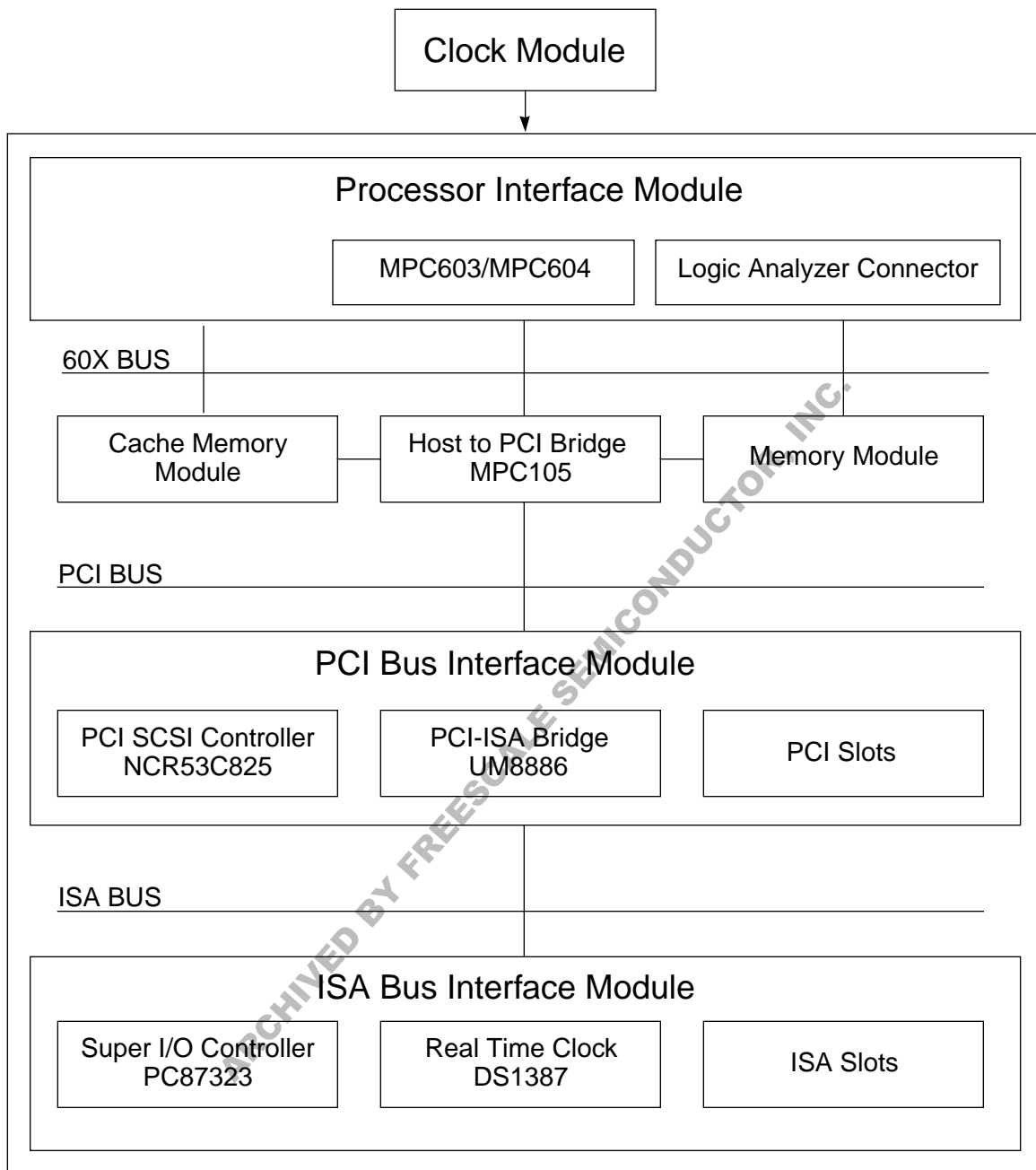


Figure 1. System Block Diagram

1.3 Performance

The key goal for the Big Bend design is high performance at a reasonable cost.

The following timing indicates the number of clock cycles the MPC105 takes for different operations. It is based on the 66-MHz processor bus frequency, 33-MHz PCI frequency, 64-bit 60X bus and 60-ns DRAM and 1 Mbyte of L2 cache with a 9-ns access time; see Table 1.

Table 1. Performance Analysis

Processor to Memory	
L2 Cache Hit	Number of Cycles
Burst read	3-1-1-1
Burst write	3-1-1-1
Read followed by pipelined write	3-1-1-1-2-1-1-1
PCI to Memory	
L2 Cache Hit	Number of Cycles
Burst write	2-1-1-1-1-1-1-1
On-Chip Cache (MPC603/MPC604) and L2 Miss	Number of Cycles
Burst read	9-1-1-1-1-1-1-1
Burst write	2-1-1-1-1-1-1-1
Processor to PCI	
Burst read	12-2-2-2

1.4 Hardware Overview

The system block diagram shown in Figure 1 has seven modules that are now described in turn.

- Clock module
- Processor interface module
- Host to PCI bridge
- Memory module
- Cache memory module
- PCI bus interface module
- ISA bus interface module

1.4.1 Clock Module

Figure 2 shows the clock module on the Big Bend system.

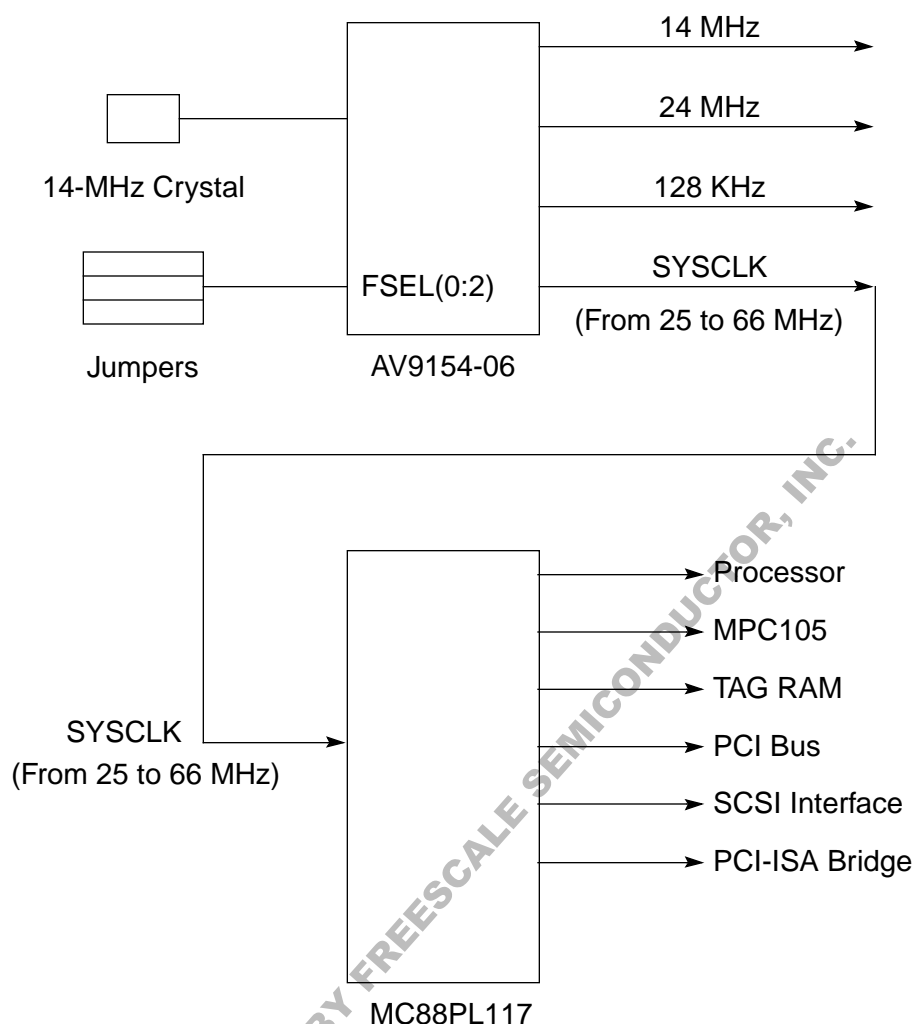


Figure 2. Clock Module

There are two clock drivers on the Big Bend system—the ICS AV9154-06 and the Motorola MC88PL117. The AV9154-06 uses an external 14.31818 MHz crystal input. External jumpers tied to the FSEL(0:2) inputs on the AV9154-06 determine the SYSCLK frequency (25 MHz–66 MHz), which drive the MC88PL117. MC88PL117 uses the SYSCLK input to generate the required frequencies for the processor, the MPC105, the TAG RAM, the PCI bus, the SCSI interface, and the PCI-ISA bridge. The AV9154-06 also generates the clock signal required for the super I/O chip, the OSC signal on the ISA bus, and also a 128-KHz signal for the suspend refresh mode of the MPC105. The MC88PL117 utilizes an internal phase-locked loop to create multiple frequencies, and has low-skew, large fan-out driving capability. The MC88PL117 has a total of 14 high current outputs with output frequencies referenced to the SYSCLK frequency. Table 2 shows the frequencies that are used in the Big Bend system.

Table 2. Supported Frequencies

MPC603/MPC604		MPC105		PCI Bus Clock
External Clock Frequency	Internal Clock Frequency	External Clock Frequency	Internal Clock Frequency	
40 MHz	80 MHz	20 MHz	40 MHz	20 MHz
25 MHz	75 MHz ¹	25 MHz	25 MHz	25 MHz
33 MHz	66 MHz	33 MHz	33 MHz	33 MHz
33 MHz	100 MHz ²	33 MHz	66 MHz	33 MHz
66 MHz	66 MHz	33 MHz	66 MHz	33MHz
66 MHz	100 MHz	33 MHz	66 MHz	33 MHz

¹ 80-MHz processor operating at 75 MHz

² PowerPC 604™ microprocessor only

1.4.2 Processor Interface Module

Figure 3 shows the processor interface module system.

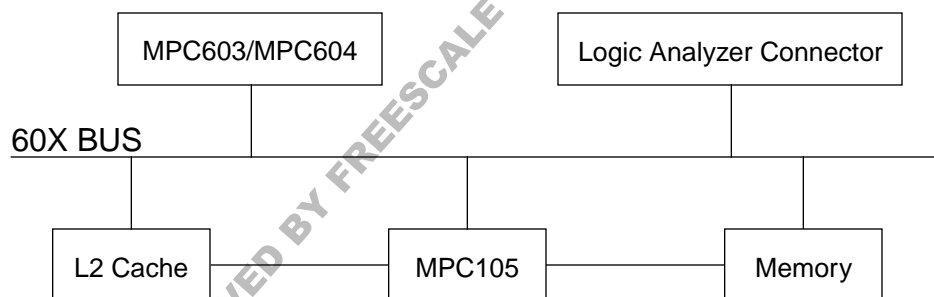


Figure 3. Processor Interface Module

The MPC603 or MPC604 processor generates the internal operating frequency using internal phase-locked loop circuitry. The MPC603 has the x1, x2, x3, and x4 options and the MPC604 has the x1, x1.5, x2, and x4 options. These options are controlled through the PLL (0:3) signals. Refer to the MPC603 and MPC604 user's manuals for more information on each of these settings. Jumpers are provided on the Big Bend motherboard to configure the PLL (0:3) pins. The PLL(0:3) pins should be configured for the desired frequency prior to power-up.

A 160-pin logic analyzer connector is located onboard for debugging purposes.

1.4.3 Host to PCI Bridge Module

Figure 4 shows the block diagram of the MPC105.

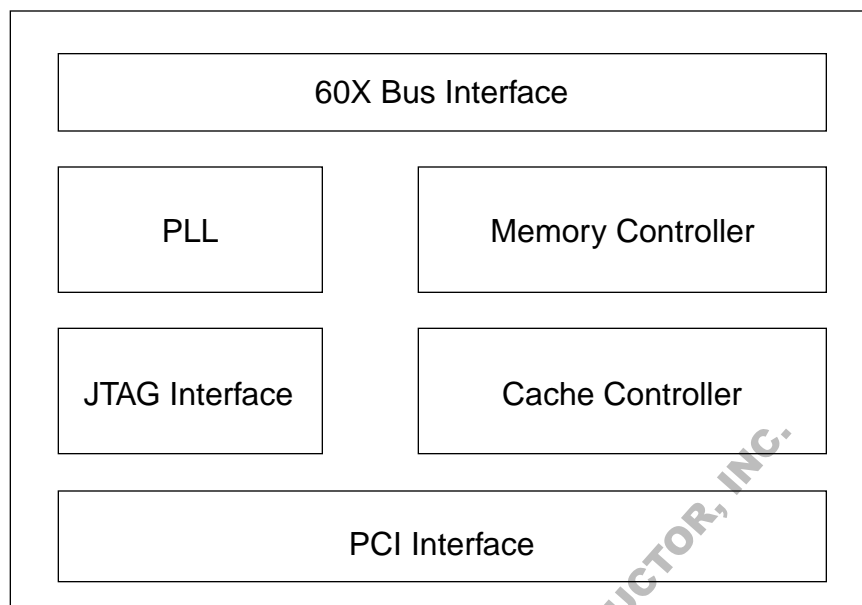


Figure 4. MPC105 Block Diagram

The MPC105 is the single-chip PReP compliant bridge device providing access between the MPC603/MPC604 processor and the PCI bus. MPC105 also integrates a secondary cache controller and a high performance memory controller that supports DRAM or SDRAM, and ROM or Flash ROM. In the Big Bend design, up to 128 Mbytes of onboard DRAM and 1 Mbyte of Flash ROM are supported. The MPC105's processor interface module handles the processor transactions and performs snoop operations. This interface also provides the bus arbitration function between the processors, one level of address pipelining, and address and data bus parking. The secondary cache controller supports 256 Kbyte to 1 Mbyte of direct-mapped cache in write-through or write-back mode; either mode can be programmed through an internal configuration register. For performance reasons, Big Bend supports the write-back mode as the default.

The MPC105 starts both secondary cache and memory accesses in parallel to reduce secondary cache miss latency. The memory cycle is aborted if there is a hit on the second-level cache. Nonpipelined burst transactions can be completed with a timing of 3-1-1-1 clock cycles. Pipeline burst can be completed with timing of 2-1-1-1 clock cycles. The cache controller interfaces with external TAG RAM and synchronous RAM. Programmable timing is provided to suit various system requirements.

The JTAG interface on the MPC105 provides a boundary-scan capability for board testing. The MPC105 provides all the test port signals required by the IEEE 1149.1 boundary-scan specification. For more information about JTAG, refer to the IEEE 1149.1 document.

1.4.4 Memory Interface Modules

Figure 5 shows the memory module on the Big Bend system.

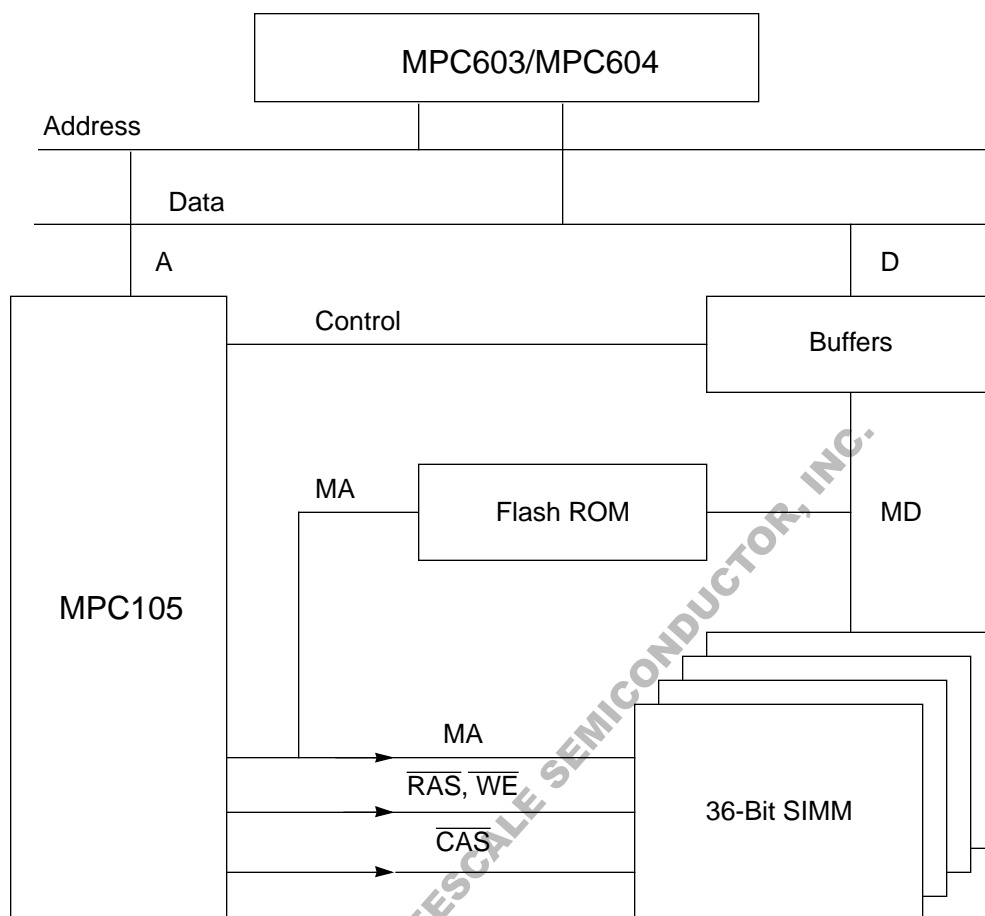


Figure 5. Memory Module on Big Bend

The MPC105's memory interface module is designed to support DRAM or synchronous DRAM as main memory. Big Bend supports 4 banks of DRAM with a maximum of 128 Mbytes when using 16-Mbit RAM. Bidirectional buffers are needed on the data bus. The enable and direction control are managed by the MPC105. Buffers are added on all the MA, $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ signals. The MPC105 supports normal $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh. In sleep mode, the MPC105 uses the 128-KHz clock as a refresh time base. The best case access timing using 60-ns DRAMs at 66 MHz is 7-3-3-3 clock cycles.

The MPC105's memory interface module is also designed to support ROM or Flash ROM on either the 60X bus or the PCI bus. Big Bend supports Flash ROM for easy code update. A 512-Kbyte Flash ROM is located on the 60X Bus.

1.4.5 Cache Memory Module

Figure 6 shows the cache memory module on the Big Bend system.

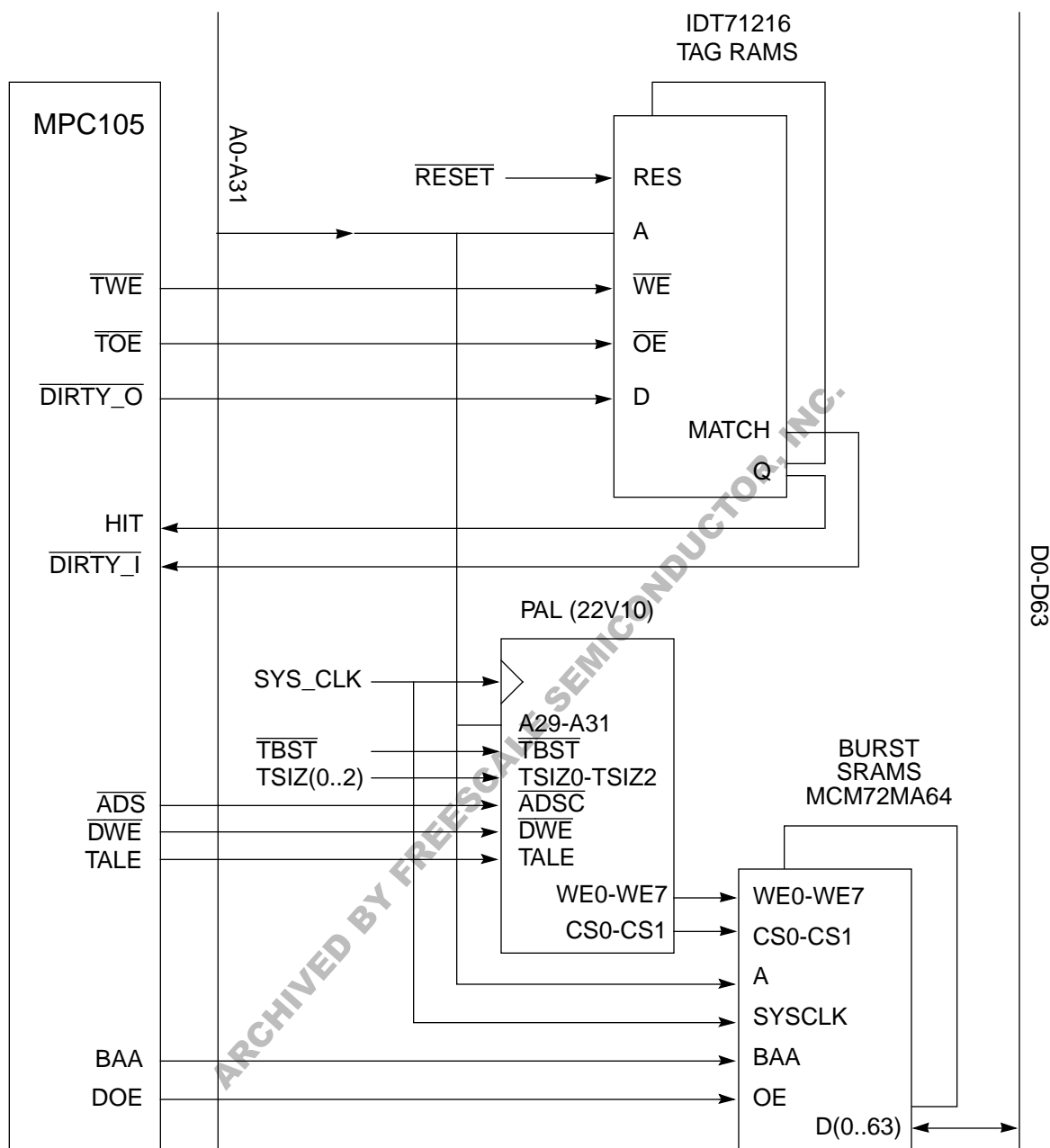


Figure 6. Cache Memory Module

Big Bend supports cache sizes from 256 Kbyte to 1 Mbyte. The cache interface circuitry inside the MPC105 is designed to run at 66 MHz. IDT 71216 16K x 15 TAG RAMs and Motorola MCM72MA64 burst SRAMs are used as the data synchronous RAM. The access time is 10 ns for TAG RAM and 9 ns for the data SRAMs. Big Bend supports both write-back and write-through direct-mapped operation. The fastest nonpipelined burst cycle is 3-1-1-1 while the timing for pipelined bursts is 2-1-1-1. The MPC105 provides four signals for interfacing the synchronous burst SRAMs. External logic (22V10 PAL) is required in the Big Bend system to decode which bytes of the 64-bit double word should be selected for the write by decoding the $\overline{A29-A31}$, \overline{TBST} , and the $\overline{TSIZ0-TSIZ2}$ signals. Currently, parity on the secondary-level cache is not supported.

1.4.6 PCI Interface Module

Figure 7 shows the PCI interface module on the Big Bend system.

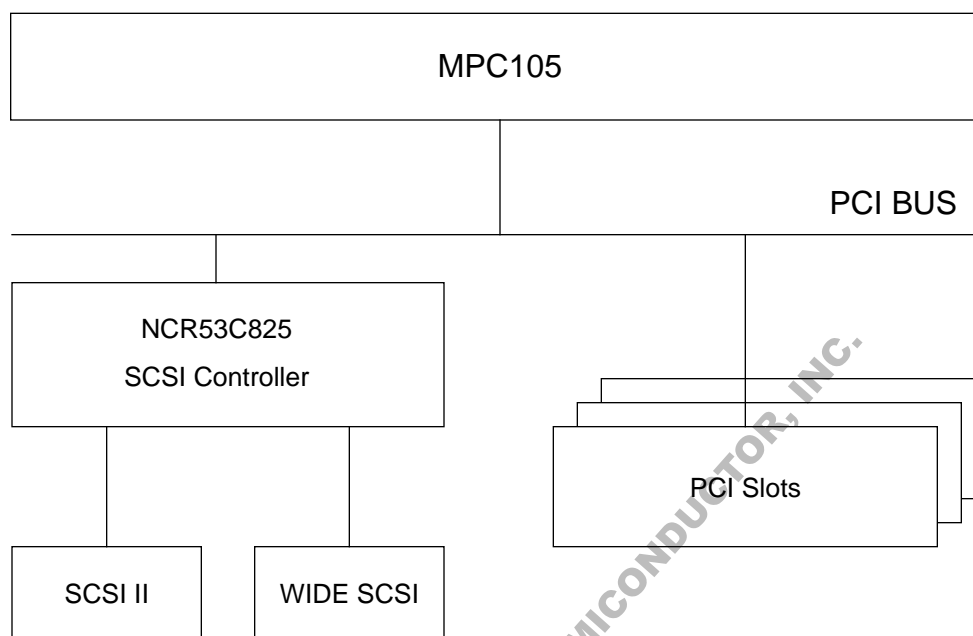


Figure 7. PCI Interface Module

There are three PCI slots available on the Big Bend system. One slot is dedicated to the graphics controller card and two slots are available for other add-on cards. The MPC105 supports a 32-bit multiplexed, address/data bus that can run from 20 MHz to 33 MHz (Table 2). The MPC105 PCI interface is compliant with the PCI Local Bus Specification, revision 2.0. It also provides buffers between the PCI bus, processor, and memory to improve system performance. The MPC105 implements two 16-byte processor-to-PCI write buffers. These buffers are split to allow the store gathering function defined in the PCI specification. Store gathering is important for high performance graphic frame buffer operations in which a whole sequence of consecutive writes can be generated by the software. One 32-bit processor-to-PCI read buffer is also implemented. Data in this buffer is not forwarded to the processor until the buffer is full or the transaction is completed. Between system memory and PCI, the MPC105 implements two 32-byte PCI-to-memory write buffers. These buffers hold two cache lines so that back-to-back writes from PCI may occur, with PCI filling one buffer while the data in the other is forwarded to system memory. One 32-byte PCI-to-memory read prefetch buffer is also implemented. The MPC105 supports speculative read operation while it prefetches the next cache line at the completion of the first PCI read operation to enhance the PCI-to-memory read performance.

The SCSI interface is provided by an NCR53C825 PCI SCSI controller. It supports both the 8-bit SCSI II interface and the 16-bit wide SCSI interface (both connectors are located on the Big Bend system). Both the CD ROM and the hard disk in the Big Bend system are accessed via the SCSI interface.

1.4.7 ISA Bus Interface Module

Figure 8 shows the ISA bus interface module.

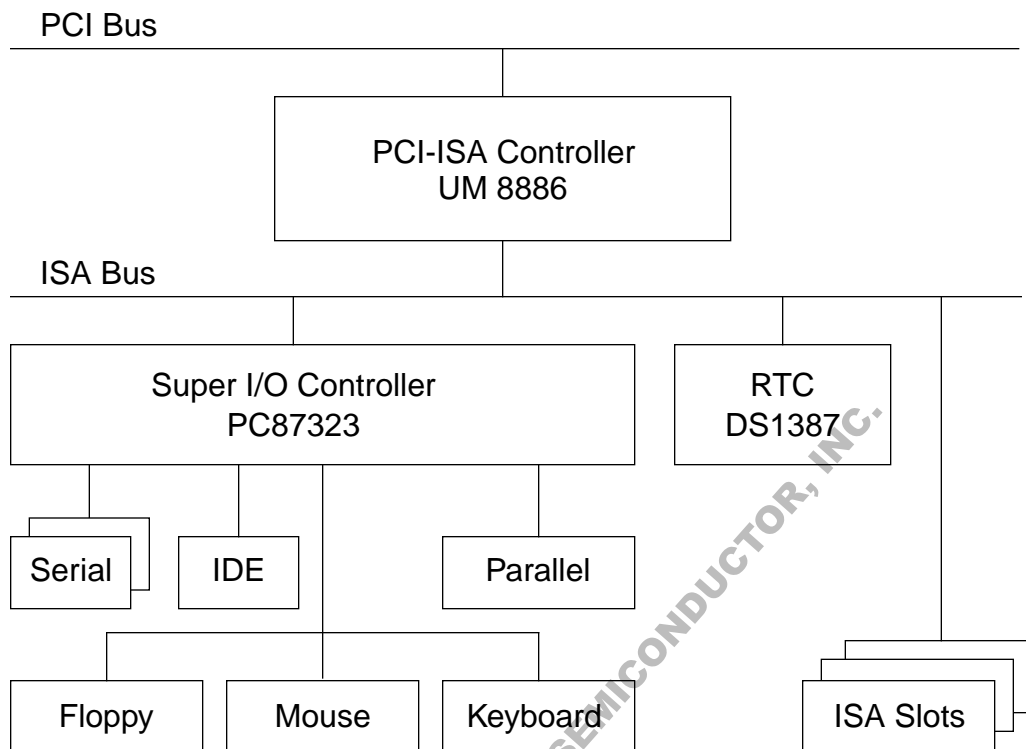


Figure 8. ISA Bus Interface Module

Big Bend uses the UMC UM8886 PCI-ISA controller as a bridge to the ISA bus. The UM8886 provides the following functions:

- 100% PCI and ISA compatible
- Incorporates two 8237 DMA controllers
- High performance PCI arbiter
- Incorporates two 8259 interrupt controllers
- One 82C54 16-bit counter/timer

Big Bend uses the National PC87323 super I/O controller to provide the functionality of two(16550 UART-compatible) serial ports, one bidirectional parallel port, an 8042 compatible keyboard controller, a PS/2-style keyboard and mouse interface, an 82077 compatible floppy disk controller interface, and an IDE interface.

The PC87323 is connected to the ISA bus.

The real time clock function is provided by the Dallas Semiconductor DS1387 controller. It also contains a 4K nonvolatile RAM for storing system configuration data.

Three ISA slots are located on the Big Bend system. Each can support a standard 8-bit or 16-bit ISA add-on card.

1.5 Firmware

The Big Bend firmware is provided by the Motorola RISC Software division. The firmware performs the following tasks:

- Initializes chipset registers
- Tests motherboard hardware
- Performs memory sizing
- Initializes the interrupt controller
- Configures the PCI interface card
- Initializes console to text mode
- Initializes boot device
- Loads and executes the OS loader

1.6 System Configuration

The following list provides the standard system configuration for Big Bend:

- 80-MHz MPC603 PowerPC microprocessor
- 32-Mbyte memory on board
- 3.5-inch and 5.25-inch diskette drives
- 500-Mbyte SCSI hard drive
- CD ROM drive with SCSI II interface
- Windows accelerated video card w/4-Mbyte VRAM
- Ethernet card
- Baby-AT desktop case
- Three 16-bit ISA slots
- Three PCI slots
- PS/2-style keyboard and mouse
- Windows NT operating system pre-installed

1.7 Documentation

Big Bend is shipped with an evaluation kit and a manufacturing kit, which contain the following documentation:

The evaluation kit contains the following documents:

- MPC105 technical summary
- MPC603 power management application note
- MPC603 technical summary
- MPC604 technical summary
- Big Bend technical summary
- Bill of materials
- Schematics—hard copy

The manufacturing kit contains the following documents:

- MPC105 user's manual
- MPC603/MPC604/MPC105 errata sheets
- Artwork—hard copy
- Ball-grid array socket information
- Big Bend user's manual
- Board layout and wiring guidelines
- Data sheets for other components
- Gerber file
- PReP specification
- Schematics—soft copy
- Schematics component library—soft copy

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